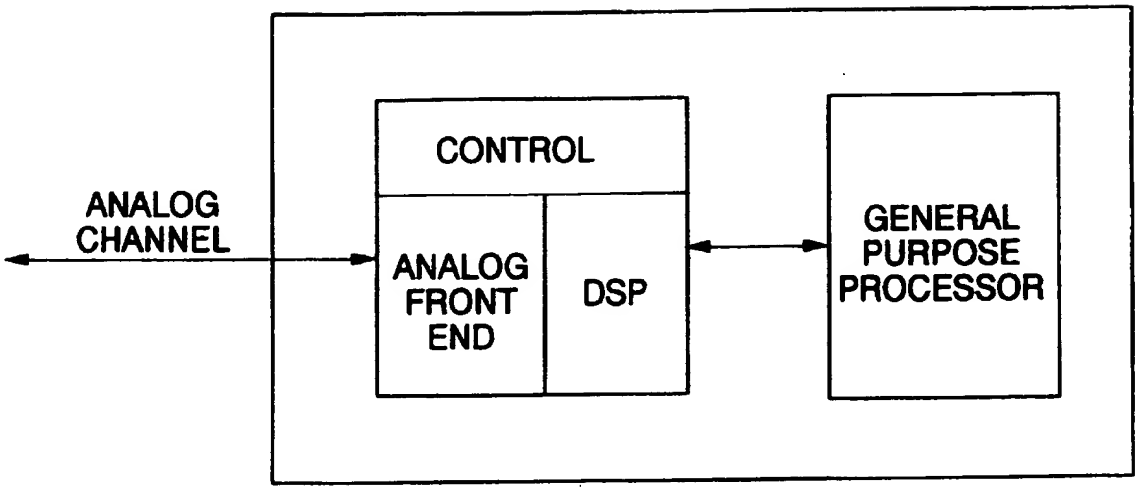

(PRIOR ART)
FIG. 1

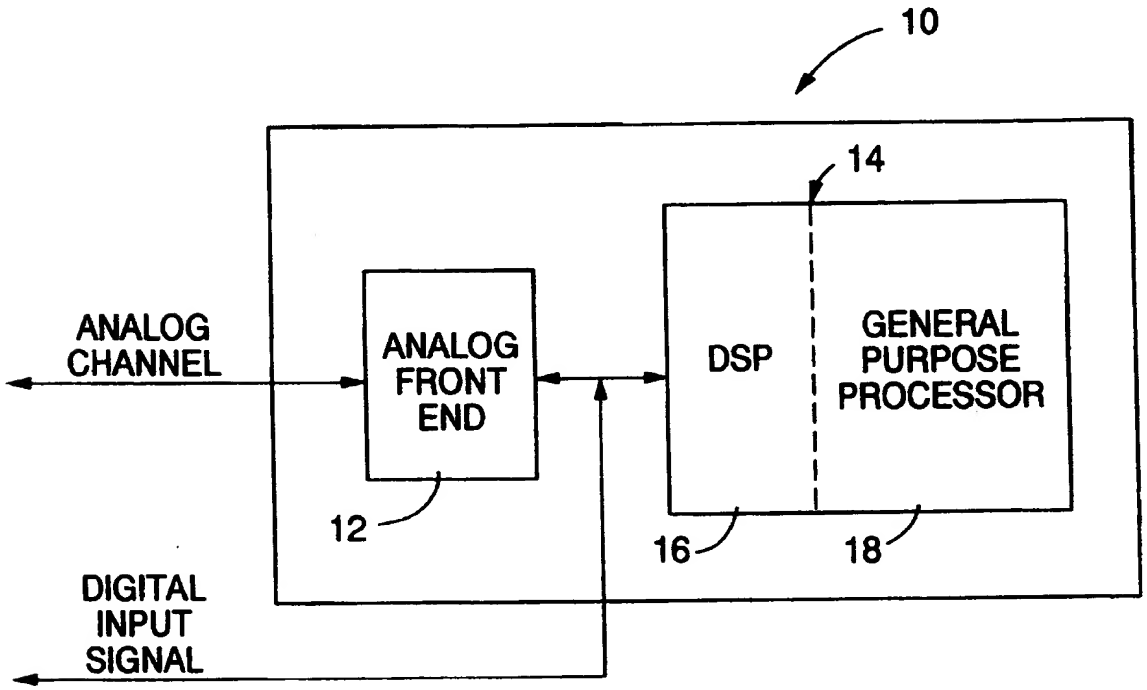

FIG. 2

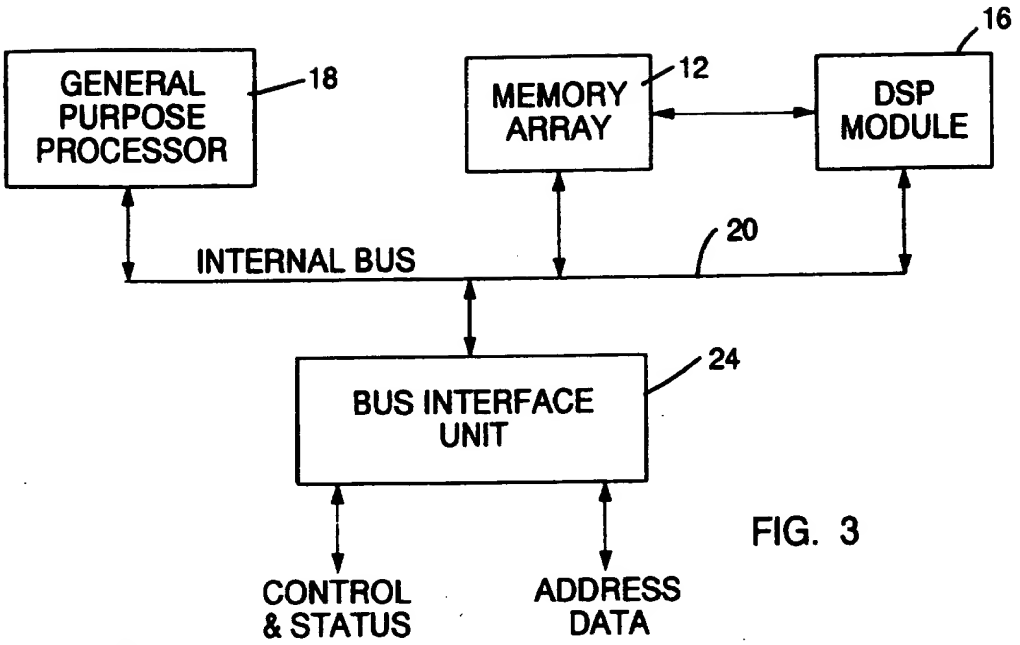

FIG. 3

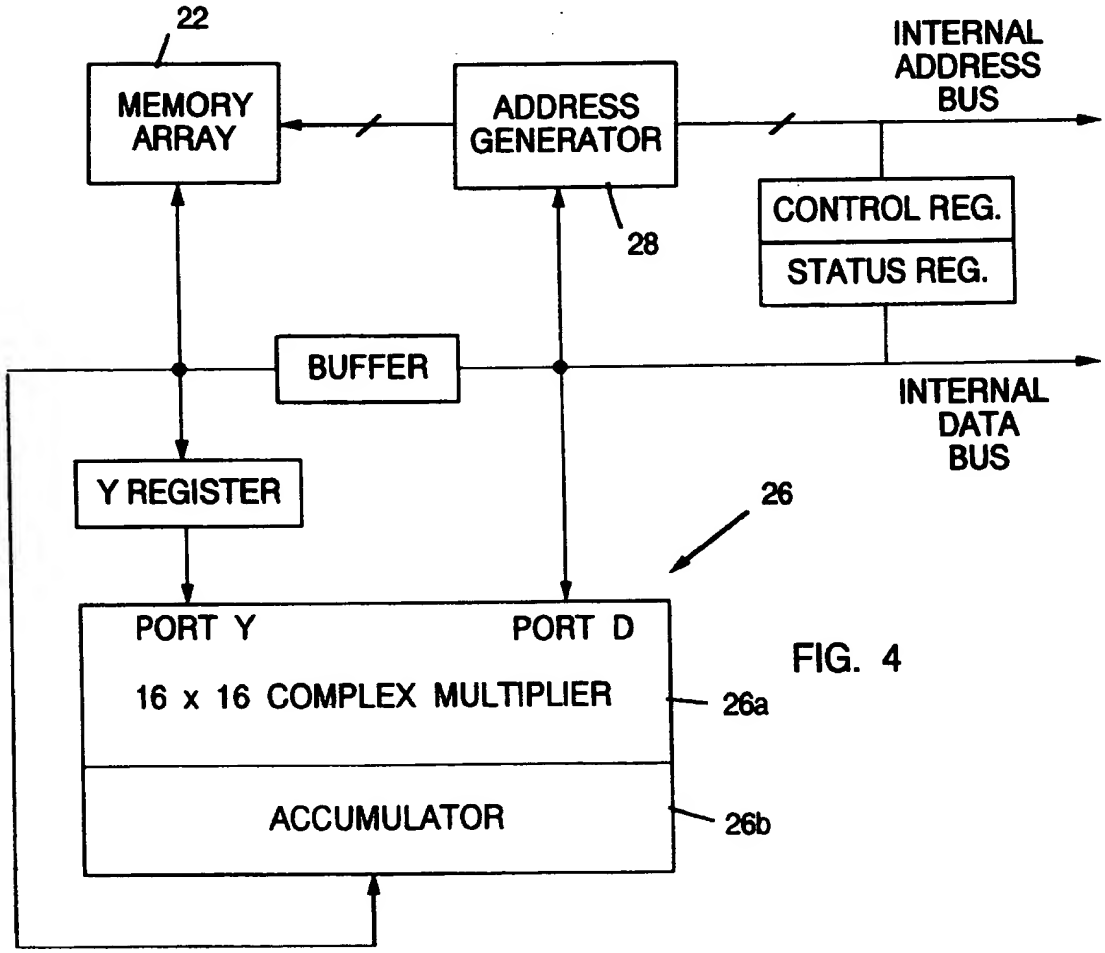

FIG. 4

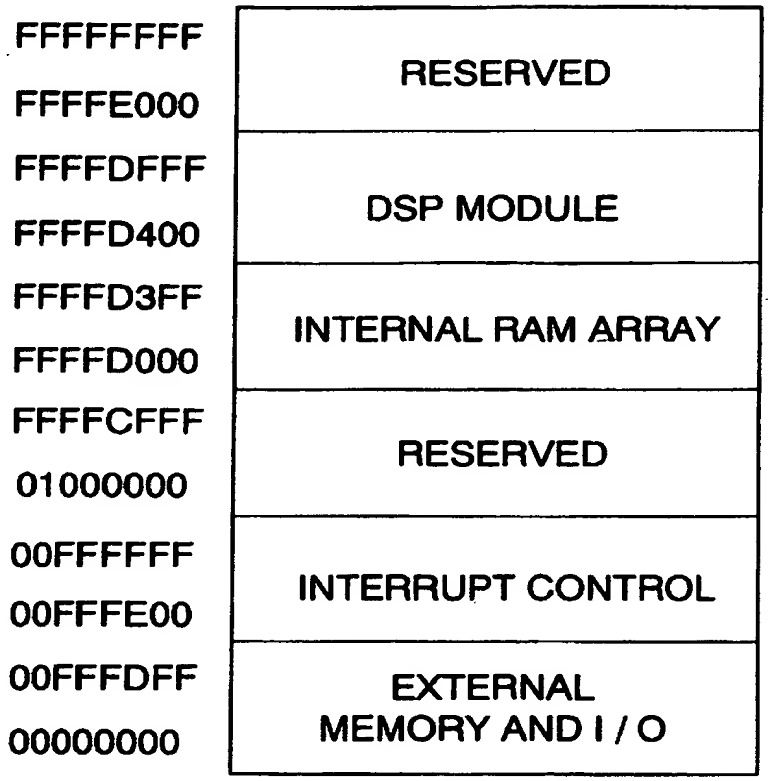

FIG. 5

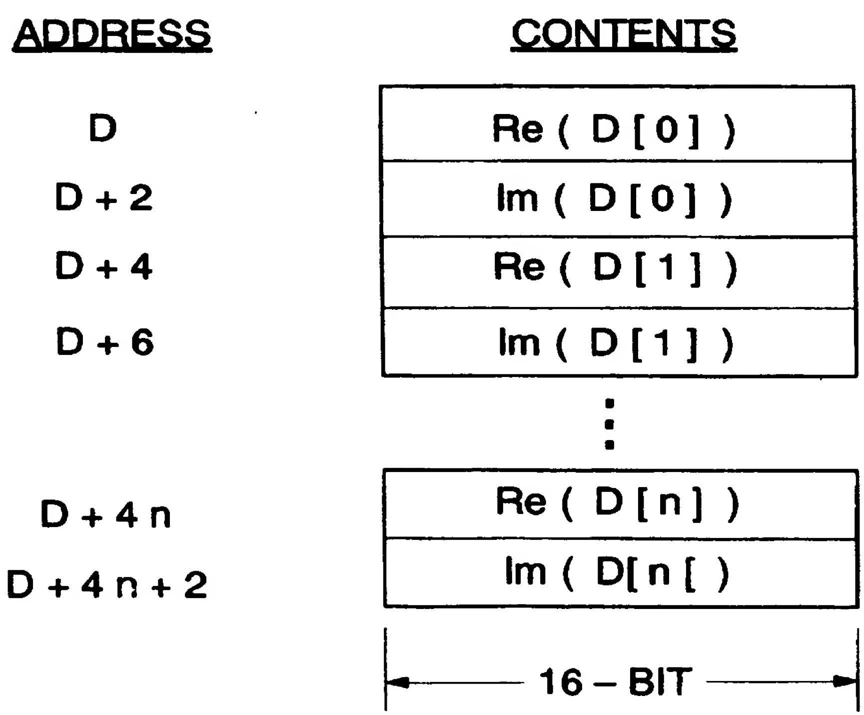

FIG. 6

INSTRUCTION	OPC1	OPC0	CLR	COJ	OPERATION	CYCLES
VCMAD	0	0	0	0	C[i] <= C[i] + Y x D[i]	9 + (N x 8)
	0	0	0	1	C[i] <= C[i] + Y x D[i] *	
	0	0	1	0	C[i] <= Y x D[i]	
	0	0	1	1	C[i] <= Y x D[i]*	
VCMUL	0	1	0	0	C[i] <= C[i] x (1 + D[i])	9 + (N x 8)
	0	1	0	1	C[i] <= C[i] x (1 + D[i]*)	
	0	1	1	0	C[i] <= C[i] x D[i]	
	0	1	1	1	C[i] <= C[i] x D[i]*	
VCMAC	1	0	0	0	A <= A + SIGMA (C[i] x D[i])	6 + (N x 8)
	1	0	0	0	A <= A + SIGMA (C[i] x D[i]*)	
	1	0	1	0	A <= SIGMA (C[i] x D[i])	
	1	0	1	1	A <= SIGMA (C[i] x D[i]*)	
VCMAG	1	1	0	0	A <= A + SIGMA (C[i] x C[i])	5 + (N x 8)
	1	1	0	1	A <= A + SIGMA (C[i] x C[i]*)	
	1	1	1	0	A <= SIGMA (C[i] x C[i])	
	1	1	1	1	A <= SIGMA (C[i] x C[i]*)	

FIG. 7

DS1	DS0	EXTERNAL BUFFER SIZE (DM)	CONSTANT ADDRESS BITS	INCREMENTED ADDRESS BITS
0	0	8	A0 , A5 – A23	A1 – A4
0	1	16	A0 , A6 – A23	A1 – A5
1	0	32	A0 , A7 – A23	A1 – A6
1	1	64	A0 , A8 – A23	A1 – A7

FIG. 8

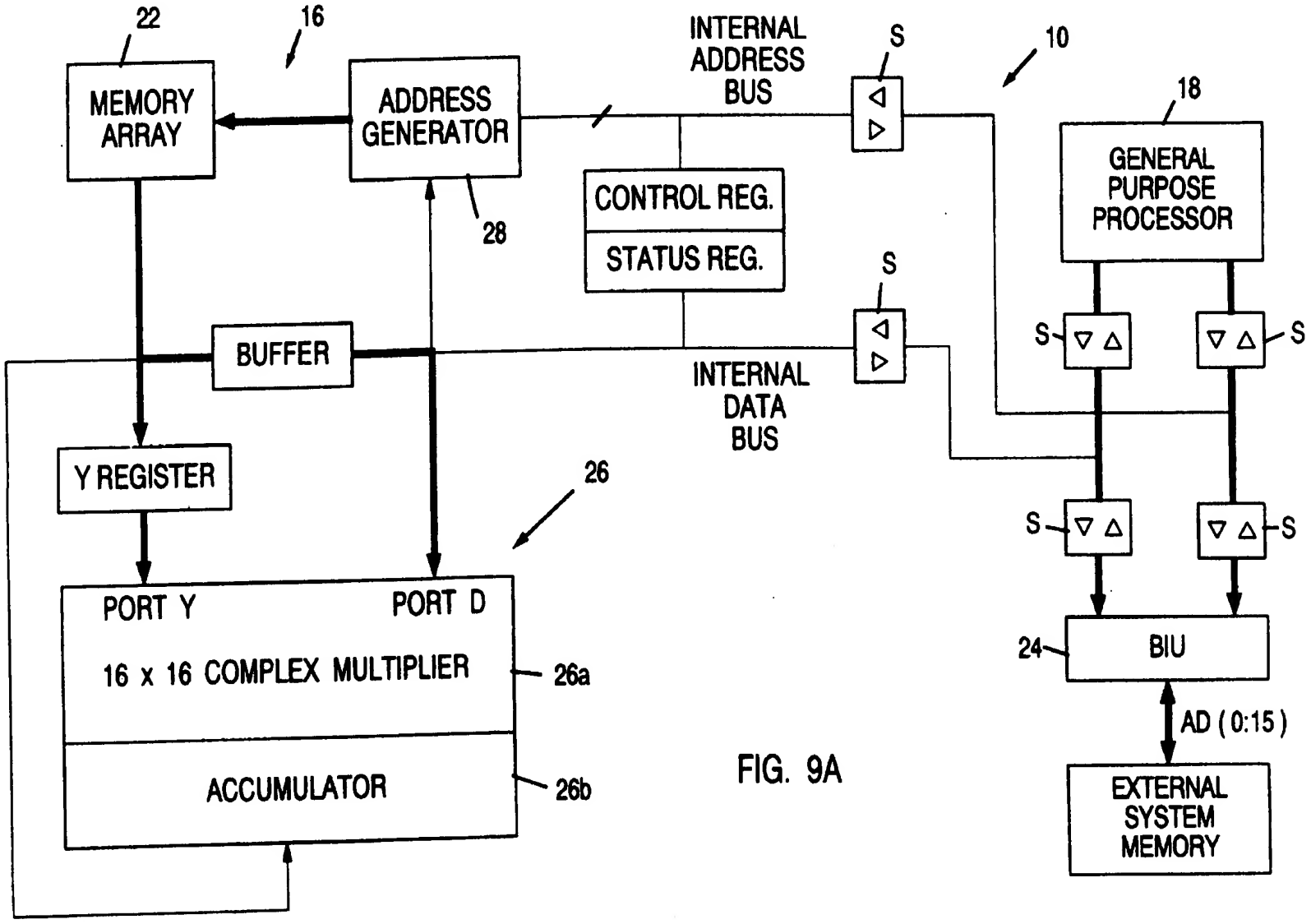

FIG. 9A

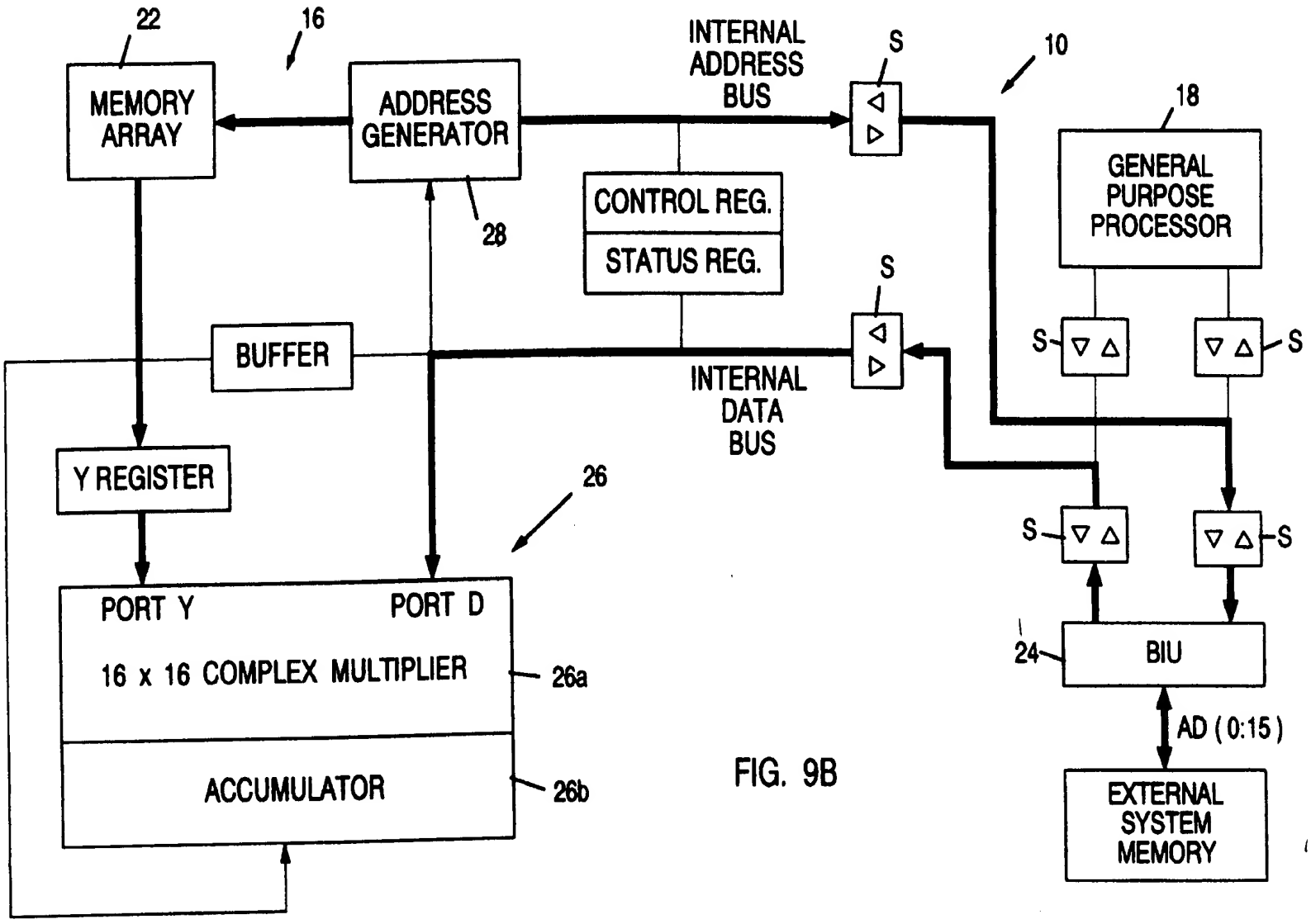

FIG. 9B

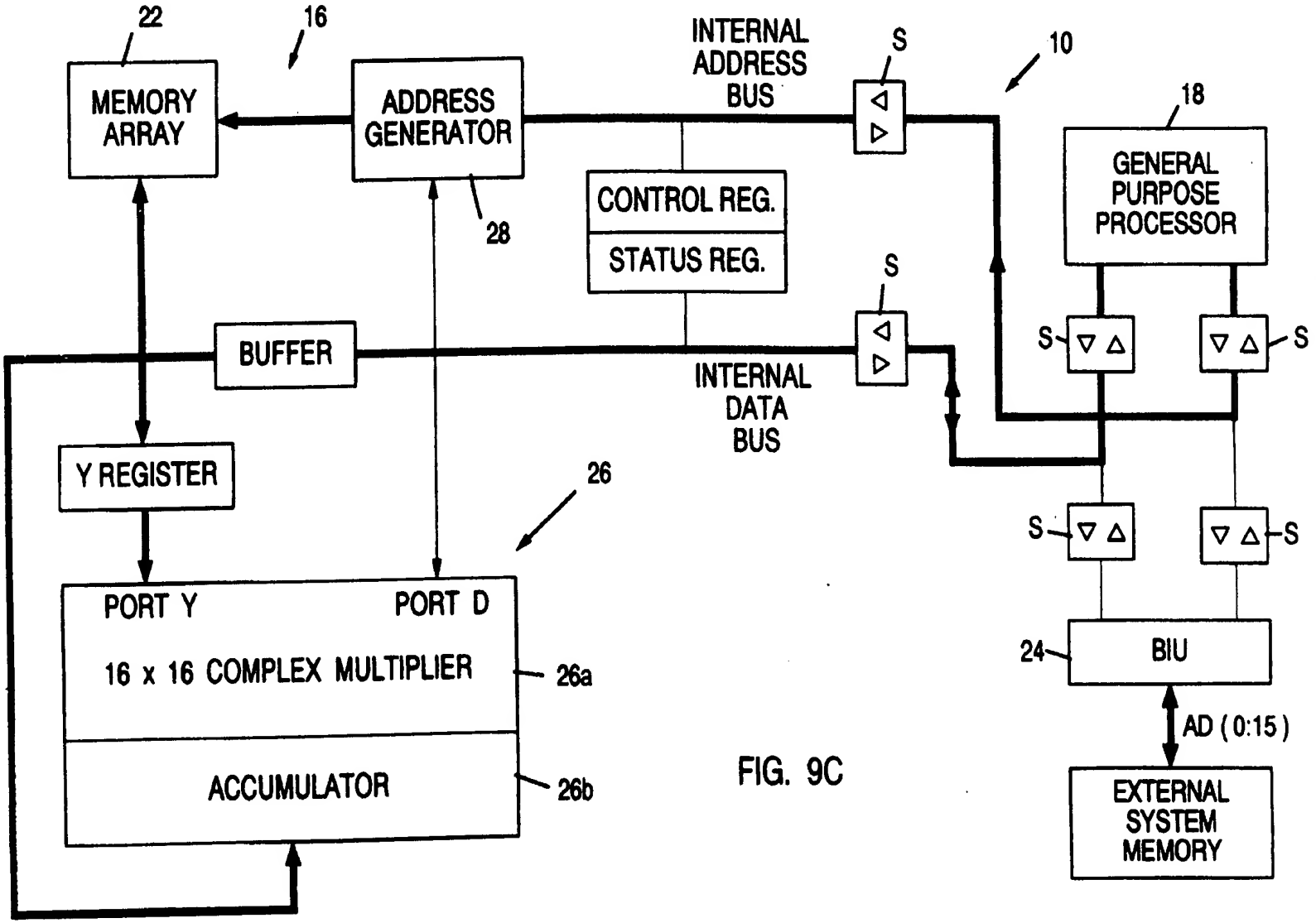

FIG. 9C